AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) An array substrate for use in a liquid crystal display device, comprising:

a gate electrode and a gate line, each having a molybdenum alloy (Mo-alloy) layer including one of tungsten (W), neodymium (Nd), niobium (Nb) and the combination thereof and a copper (Cu) layer ~~configured sequentially~~ on a substrate,

wherein the Mo-alloy layer is formed on the substrate and the Cu layer is formed on the Mo-alloy layer;

a gate insulation layer on the substrate to cover the gate electrode and the gate line;

an active layer arranged on the gate insulation layer in a portion over the gate electrode;

an ohmic contact layer on the active layer;

a data line on the gate insulation layer, the data line crossing the gate line and defining a pixel region;

source and drain electrodes on the ohmic contact layer, the source electrode extending from the data line, and the drain electrode spaced apart from the source electrode;

a passivation layer on the gate insulation layer covering the data line and the source and drain electrodes, the passivation layer having a drain contact hole exposing a portion of the drain electrode; and

a pixel electrode configured on the passivation layer in the pixel region, the pixel electrode electrically contacting the drain electrode through the drain contact hole.

2. (Cancelled)

3. (Original) The substrate according to claim 1, further comprising a storage metal layer configured over a portion of the gate line.

4. (Original) The substrate according to claim 3, wherein the storage metal layer is formed with the data line on the gate insulation layer.

5. (Original) The substrate according to claim 3, wherein the pixel electrode electrically contacts the storage metal layer via a storage contact hole.

6. (Original) The substrate according to claim 3, wherein the data line, the source electrode, the drain electrode and the storage metal layer are all formed of a double-layered metal pattern consisting of a lower part of molybdenum alloy (Mo-alloy) and an upper part of copper (Cu).

7. (Original) The substrate according to claim 6, wherein the molybdenum alloy (Mo-alloy) includes one of tungsten (W), neodymium (Nd), niobium (Nb) and the combination thereof.

8. (Original) The substrate according to claim 3, wherein the data line, the source electrode, the drain electrode and the storage metal layer are all formed of a single layer of copper (Cu).

9. (Original) The substrate according to claim 1, wherein the molybdenum alloy layer of the gate electrode and gate line has a thickness in a range from about 10 to about 500 angstroms.

10. (Original) The substrate according to claim 1, wherein the copper layer has a thickness in a range from about 500 to about 5000 angstroms.

11. (Withdrawn) A method of fabricating an array substrate for used in a liquid crystal display device, comprising:

forming a molybdenum alloy (Mo-alloy) layer and a copper (Cu) layer sequentially on a substrate;

patterning the molybdenum alloy (Mo-alloy) layer and the copper (Cu) layer to form a Cu/Mo-alloy double-layered gate line and a Cu/Mo-alloy double-layered gate electrode, said gate line being disposed in a transverse direction and said gate electrode extending from the gate line;

forming a gate insulation layer on the substrate to cover said gate line and said gate electrode;

forming an active layer and an ohmic contact layer sequentially on the gate insulation layer, over said gate electrode;

forming a data line, a source electrode and a drain electrode, wherein the data line is disposed on the gate insulation layer and crosses the gate line to define a pixel region, the source electrode extends from the data line on the ohmic contact layer, and the drain electrode is spaced apart from the source electrode on the ohmic contact layer;

forming a passivation layer on the gate insulation layer to cover the data line, the source electrode and the drain electrode, wherein the passivation layer has a drain contact hole that exposes a portion of the drain electrode; and

forming a pixel electrode on the passivation layer, wherein the pixel electrode electrically contacts the drain electrode through the drain contact hole.

12. (Withdrawn) The method according to claim 11, wherein the gate insulation layer and the passivation layer are formed of an inorganic material selected from a group consisting of silicon oxide and silicon nitride.

13. (Withdrawn) The method according to claim 11, wherein the passivation layer is formed of an organic material selected from a group consisting of benzocyclobutene (BCB) or acrylic resin.

14. (Withdrawn) The method according to claim 11, wherein the molybdenum alloy (Mo-alloy) layer includes one of tungsten (W), neodymium (Nd), niobium (Nb) and the combination thereof.

15. (Withdrawn) The method according to claim 11, wherein forming the data line includes forming a storage metal layer over a portion of the gate line.

16. (Withdrawn) The method according to claim 15, wherein the storage metal layer is disposed on the gate insulation layer underneath the passivation layer.

17. (Withdrawn) The method according to claim 15, wherein the pixel electrode electrically contacts the storage metal layer via a storage contact hole.

18. (Withdrawn) The method according to claim 15, wherein the data line, the source electrode, the drain electrode and the storage metal layer are all formed of a double-layered metal pattern consisting of a lower part of molybdenum alloy (Mo-alloy) and an upper part of copper (Cu).

19. (Withdrawn) The method according to claim 18, wherein the molybdenum alloy (Mo-alloy) includes one of tungsten (W), neodymium (Nd), niobium (Nb) and the combination thereof.

20. (Withdrawn) The method according to claim 15, wherein the data line, the source electrode, the drain electrode and the storage metal layer are all formed of a single layer of copper (Cu).